## REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 28 July 2005. Responsive to the rejections and objections made in the Official Action, Independent Claim 1 has been amended to further clarify the combination of elements that define the invention of the subject Patent Application. Also, Claims 3-4, 6 -8 and 10 have been amended to remove informalities found therein and to improve the claim language thereof.

In the Official Action, the Examiner objected to Claims 7, 8 and 10 for found minor informalities. Accordingly, Claims 7, 8, and 10 have been amended as requested by the Examiner. It is believed that by the amendments to Claims 7, 8 and 10, objection of the Examiner can be lifted.

Claims 1 – 4, and 8 – 10 were rejected under 35 U.S.C. § 112 (second paragraph) for failing to point out and distinctly claim the subject matter which the Applicant regards as the invention. Accordingly, Claims 1 and 8 have been amended to overcome the second paragraph of 35 U.S.C. § 112 rejection.

Further, in the Official Action, the Examiner rejected Claim 1 under 35 U.S.C. § 102(e) as being anticipated by Imamura et al., U.S. Patent 6,476,503 B1; Claims 5 – 6, and 8 were rejected under 35 U.S.C. § 102(e) as being anticipated by Sakuyama et al., U.S. Patent 6,580,169 B2; Claims 2 – 4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Imamura et al. in view of Horiuchi et

al., U.S. Patent 6,731,010 B2; Claims 7 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakuyama et al. in view of Horiuchi et al.; and Claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakuyama et al. in view of Imamura et al. and further in view of Horiuchi et al.

With regard to Claim 1, the Examiner stated that Imamura et al. disclosed a semiconductor image sense chip 14, a conducting wire 16 extending from each of the multiple bonding pads 23, a liquefied jelly material 18b and 18a covering the top face of the semiconductor image sense chip 14 after drying up, and the transparent layer 18 having a thickness being equal to a height of each of the conduct wire 16 relative to the top face of the semiconductor image sense chip 14.

It is respectfully submitted, that Imamura et al. Patent fails to suggest, disclose or render obvious the structure which the Applicant regards as the invention. Specifically, in contrast to the present invention, in Imamura et al., the resin layer 18 is never presented as a transparent layer.

While in the present invention, the layer 13 is a transparent layer formed of a gelatinous material which is dried up to form the transparent layer 13.

Further, inn Imamura et al., the resin layer 18 consists of two or more layers such as 18a, 18b, etc. of different elasticity intended to enhance the durability of the structure to the thermal fatigue which may be caused by a repetitive generation of thermal stress which the structure of Imamura et al. undergoes.

While in the present invention, in contradistinction to Imamura et al., the transparent layer 13 is a single layer structure formed of a single liquefied gelatinous material.

Claim 1 as amended, clearly limits itself to (inter alia):

"... a transparent layer on the top face of the semi-conductor image sense chip ..." and

"... transparent layer being a single layer structure ...".

As the Imamura et al. Patent fails to disclose each and every one of the claimed elements, it cannot anticipate the invention of the subject Patent Application as now claimed in the independent Claim 1. Therefore, the allowance of Claim 1, as amended, is believed; and the same is respectfully requested.

Sakuyama et al., the reference cited against Independent Claim 5, is directed to a method for forming bumps in which the mask 2 having openings corresponding to the electrode pads is formed on the top of the chip, and is removed after the bumps B are formed in the openings, as shown in Figures 5a – 5d.

The Examiner stated that Sakuyama et al. discloses a semiconductor image sense chip 1, having multiple bumps B formed on a top face of the semiconductor image sense chip 1, the transparent layer 2 attached to the top face of the semiconductor image sense chip 1, wherein the transparent layer 2 has a thickness being equal to that of each of the bumps B.

It is respectfully submitted, that the layer 2 is merely a mask which serves for forming bumps B in the openings thereof and which is removed once the bumps have been formed. In contradistinction to the present invention, the mask 2 is not a transparent layer and does not constitute a part of the entire semiconductor device package since it is removed therefrom.

While in the present invention, the transparent layer 13 is permanently attached to the top face of the semiconductor image sense chip and is not removed therefrom since it constitutes a portion of the entire chip scale package structure.

Claim 5 limits itself (inter alia) to:

"... a transparent layer attached to the top face of the semi-conductor image sense chip ...".

This feature is not shown in Sakuyama et al. Therefore, as Sakuyama et al. reference fails to disclose each and every one of the claimed elements, it cannot anticipate the invention of the subject Patent Application, as claimed in Independent Claim 5. Accordingly, the allowance of Claim 5 is believed; and the same is respectfully requested.

The Examiner cited the Horiuchi et al. Patent for disclosing a shelter 30, a flexible printed circuit board 23 having a window formed therein and as disclosing pin wires, the elements the Imamura et al. Patent fails to disclose. The Examiner concludes that it would have been obvious to one of ordinary skilled in the art at the time the invention was made, to modify Imamura et al. to have a shelter 30

disclosed by Horiuchi et al. in the rejection of Claim 2; or to modify Imamura et al. to have a flexible printed circuit board with a window in rejection of Claim 3; or to modify the Imamura et al. to have pin wires in the rejection of Claim 4 of Horiuchi et al.

Further, the Examiner suggests to modify Sakuyama et al. with a flexible printed circuit board having a window of Horiuchi et al. in the rejection of Claims 7 and 10. Also, the Examiner suggests that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sakuyama et al. with the teaching of Imamura et al. (disclosing an inherent top face ground and burnished) and Horiuchi et al. disclosing a shelter 30 in the rejection of Claim 9.

Horiuchi et al. relates to a thin package semiconductor device which includes a printed circuit board 23 provided with an interconnection pattern 22 on its top surface 23A and a semiconductor ship 25 housed inside a through hole 24. The electrode terminals 25E are connected with the interconnection pattern 22 by the bonding wires 26. Sealing resin layer 27 integrally seals the bonding wires 26 and the semiconductor chip 25 and fixes the semiconductor chip 25 inside the through hole 2. The bottom surface of the printed circuit board 23 faces the back surface of the semiconductor chip 25 and the bottom surface of the sealing resin layer 27. Solder balls 28 are formed as external connection terminals at predetermined positions of the interconnection pattern 22. The other portions of

the semiconductor pattern 22 are covered by solder resist layer 29. The outer edges of the sealing resin layer 27 are defined by a dam bar 30 formed by a resin.

It is respectfully submitted that in contradistinction to the present invention, in Horiuchi et al., resin layer 27 is not a transparent layer while in the present invention the layer 13 is a transparent layer.

Further, in Horiuchi et al. thickness of the resin layer 27 is not equal to a height of the conducting wire penetrating the same.

While in the present invention, the transparent layer 13 has a thickness equal to a height of each of the conducting wire 12 or to that of each of the bumps 21 shown in Figure 5.

It is respectfully submitted, that the combination of Imamura et al. with Horiuchi et al., or Sakuyama et al. with Horiuchi et al., or Imamura et al. with Sakuyama et al. and Horiuchi et al. fails to teach, suggest or render obvious a transparent layer formed on the top face of the semiconductor image sense chip, as clearly emphasized in Independent Claims 1 and 5. Therefore, the combination of the Imamura et al., Sakuyama et al. and Horiuchi et al. in any order, cannot make obvious the invention of the subject Patent Application, as now claimed in Claims 1 and 5.

Claims 2 – 4 dependent on Claim 1, and Claims 6 – 10 dependent on Claim 5 are believed to add further limitations that are patentably distinct in addition to

being dependent upon what is now believed to be patentable base claims, and therefore, allowable for at least the same reasons.

For all of the foregoing reasons, it is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
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Dated: 24 Oct. 2005

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